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METHOD FOR PROGRAMMING, ERASING AND READING A FLASH MEMORY CELL

Abstract

A method for programming PMOS single transistor flash memory cells through channel hot carrier induced hot electron injection mechanism is disclosed. The PMOS single transistor flash memory cell includes an ONO stack layer situated on an N-well of a semiconductor substrate, a P^+ poly gate formed on the ONO stack layer, a P^+ doped source region disposed in the N-well at one side of the gate, and a P^+ doped drain region disposed in the N-well at the other side of the gate. The method includes the steps of: applying a word line voltage V_{WL} on the P^+ poly gate, applying a source line voltage V_{SL} on the source, wherein the source line voltage V_{SL} is greater than the word line voltage V_{WL}, thereby providing adequate bias to turn on the P channel thereof. A bit line voltage that is smaller than the source line voltage V_{SL} is applied on the P^+ doped drain region, thereby driving channel hot holes to flow toward the P^+ doped drain region and then inducing hot electron injection near the drain side. A well voltage V_{NW} is applied to the N-well, wherein $V_{NW}=V_{SL}$.